

In the Specification:

page 8, lines 4-8

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1 FIG. 2A shows general implementation of present interconnect
2 scheme, whereupon various endpoints 2(1), 2(2), . . . , 2(N) are flexibly
3 switched and/or routed through hardware block 10. Preferable, at least
4 one improved endpoint is provided with serial to parallel converter circuit
5 6 or parallel to serial converter circuit 7, which each convert a multi-
6 bitwidth (e.g., 32-bits) signal for sending to or receiving from one or more
7 1-bit wide signals generated by or transmitted by multiplexers in block
8 10.